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# A TELEVISION SET FEATURING DIGITAL BAND VIDEO FREQUENCY BROADCAST RECEPTION CAPABILITIES

[Dai Shuzi Shipin Guangbo Jieshou Gongneng de Diangshiji]

Wu Lin, et al.

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PATENT APPLICATION CLAIMS /1*

1. A type of television set featuring digital band video frequency broadcast reception capabilities, which include: a TV high frequency head device, a TV IF device, a video frequency hue processing device, a TV video frequency display driver device, a TV video frequency display device, Y/C and A/V interface devices, power supply device, on-board button devices, and a remote control device. It is characterized by also including:

A DVB high frequency head device used to modulate the received DVB signal from a satellite or cable source, passing through a mixed channel modulated T/S flow to the MPEG decoder, video and audio frequency encoder, and CPU device. The control signals for said DVB high frequency processing are set by the MPEG decoder, video and audio frequency encoder, and CPU device through the $I^2C$ bus.

A MPEG decoder, video and audio frequency encoder, and CPU device used to receive the T/S stream output from the DVB high frequency head device [6]. It passes through the MPEG decoder and video and audio frequency encoder to generate a three primary color image RGB signal. It is sent to the video frequency and hue processing devices, used to receive the control signals generated by the onboard key device sent through the I/O port expansion device. Or, receive remote control signals from the remote control device. Or, receive signals from the TV part of the circuit. After determinate processing, corresponding control signals are generated and are passed through the I/O port expansion device or $I^2C$ bus to control the corresponding circuit function.

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* Number in the margin indicates pagination in the foreign text

An I/O port expansion device used to control the operation of the entire TV portion under the commands sent by the MPEG decoder, video and audio frequency encoder, and CPU device.

A DVB storage device, used to download or write programs to control the MPEG decoder, video and audio frequency encoder, CPU device, DVB, and general analog television channel information. /2

2. A type of television set featuring digital band video frequency broadcast reception capabilities according to Claim 1, characterized by: the DVB high frequency head device, MPEG decoder, video and audio frequency encoder, and CPU device, I/O port expansion device, and DVB storage device compose a "DVB control card". The corresponding circuit board also contains a "DVB control card slot".

3. A type of television set featuring digital band video frequency broadcast reception capabilities according to Claim 2, characterized by: a "television control card slot", "DVB control card slot", and $I^2C$ bus connecting the "television control card slot" and circuit board designed on the circuit board. The television control card slot" and "DVB control card slot" are electrically connected to the circuit board through control lines for television function control.

## DESCRIPTION OF THE INVENTION /1

## A TELEVISION SET FEATURING DIGITAL BAND VIDEO FREQUENCY BROADCAST RECEPTION CAPABILITIES

The present utility model relates to a type of television device, specifically a type of television that can receive digital video broadcast (DVB) programs.

Existing television sets and DVB set-top boxes are used for completely different functions. TVs are used the receive standard analog TV signals and DVB set-top boxes are used to receive digital video broadcast signals, of which after the MPEG-2 stream is digitally decoded, it is encoded as a three primary color image RGB signal, Y/C, or a full TV CVBS signal and input into the corresponding port on the TV. When a user is viewing a DVB program, two separate remote controls must be used to before the various control functions for the television set and DVB set-top box system, making operation inconvenient.

The purpose of the present utility model is to provide a type of general television set and DVB set-top box system as one unit, only needing one remote control to control a TV for digital band video frequency broadcast reception functions to overcome the aforementioned deficiencies.

The present model utility provides a television set featuring digital band video frequency broadcast, including: a TV high frequency head device for modulating the RF high frequency signal received from a standard analog television and obtaining the IF signal from the TV through mixing and filter, and sending the signal to the drive device in the television for processing; a drive device in the television to receive the IF signal output from the television high frequency head device to form the full TV image signal and sending it to the video frequency and hue processing device; a video frequency and hue processing device to process the full picture image signal from the drive device within the television, or process the image signal from the television Y/C or A/V port device and generates a three primary color image RGB signal and horizontal and field oscillation signals which are delivered to the television video /2 frequency display driver device; a television video display driver device that amplifies and processes the three primary color image RGB signal and horizontal and field oscillation signals from the video frequency and hue processing device and provides all necessary signals to the television video frequency display device; a television video frequency display device to display the three primary color image RGB signal from the television video frequency display driver device; a Y/C and A/V port device to receive corresponding signals from an external device and provide it to the television video frequency and hue processing device; a DVB high frequency head device used to modulate the received DVB signal from a satellite or cable source, passing through a mixed channel modulated T/S flow to the MPEG decoder, video and audio frequency encoder, and CPU device. The control signals for said DVB high frequency processing are set by the MPEG decoder, video and audio frequency encoder, and CPU device through the $I^2C$ bus; a MPEG decoder, video and audio frequency encoder, and CPU device used to receive the T/S flow output from the DVB high frequency head device. It passes through the MPEG decoder and video and audio frequency encoder to generate a three primary color image RGB signal. It is sent to the video frequency and hue processing devices, used to receive the control signals generated by the onboard key device sent through the I/O port expansion device. Or, receive remote control signals from the remote control device. Or, receive signals from the TV part of the circuit. After determinate processing, corresponding control signals are generate and are passed through the I/O port expansion device or $I^2C$ bus to control the corresponding circuit function; an I/O port expansion device to control the operation of the entire TV portion under the commands sent by the MPEG decoder, video and audio frequency encoder, and CPU device; a power supply device to provide each component of the television set necessary power; an onboard key device to generate a control for the corresponding pressed key; a remote control device to generate remote control signals; and a DVB storage device used to store programs and DVB and standard analog television channel information.

Because the present utility model effectively combines the digital band video frequency broadcast reception capabilities of a television /3 with a DVB set-top box and standard color television receiver, only one power supply is needed and the onboard key and remote control device is shared. Only one CPU controller one $E^2$PROM storage device are needed to complete the color television set device. Thus, greatly reducing costs for a manufacturer. For end-users, using one remote control unifies the interface for greater convenience. From a engineering technology standpoint, product groups form an organic set, eliminating redundancy, and improving the reliability of the products.

The following diagrams and preferred embodiments further describe the present utility model.

Figure 1 is a circuit structure diagram of the preferred embodiment of the present utility model.

Figure 2 is the circuit board layout diagram of the preferred embodiment of the present utility model.

Figure 3 is the circuit diagram of the preferred embodiment of the present utility model.

Figure 4 is a diagram of the I/O expansion section of the circuit of the preferred embodiment of the present utility model.

Figure 5 is the LC electromagnetic interference resistance network circuit diagram of the preferred embodiment of the present utility model.

Figure 6 is a diagram of the television controller card for changing television programs used by the preferred embodiment of the present utility model.

Figure 7 is a diagram of the DVB controller card for changing television programs used by the preferred embodiment of the present utility model.

Referring to Figure 1 and Figure 2, the present utility model provides a television set capable of receiving DVB programs. This television includes: television high frequency head device 1, television IF device 2, video frequency and hue processing device 3, television video frequency display driver device 4, television video frequency display device 5, DVB high frequency head device 6, MPEG decoder, video and audio encoder, and CPU device 7, I/O port expansion device 8, DVB storage device 9, power supply 12, onboard button device 13, remote control device 14, and Y/C and A/V port device 15. /4

In order to satisfy certain customer demand, it is able to receive DVB programming as will as standard television programming; however some customers only want to receive standard television programming. Thus, the single circuit board is designed with two types of control cards, "DVB control card" and "television control card" for a television set with varying functionality. When the "DVB control card" is selected, it can receive both DVB programming and standard television programming. When "television control card" is selected, only standard television programming can be viewed.

The "DVB control card" comprises of a DVB high frequency head device **6**, MPEG decoder, video and audio frequency encoder, and CPU device **7**, I/O port expansion device **8**, and DVB storage device **9**. The corresponding circuit board also contains a "DVB control card slot". When a "DVB control card" is inserted, the CPU of the MPEG decoder, video and audio frequency encoder, and CPU device **7** controls the secure sequence function of the entire system. The "television control card" comprises of the television CPU device **9** and TV storage device **10**. The circuit board will also have a corresponding "television control card slot". When the "television control card" is inserted, the CPU of the television CPU device **9** controls the secure sequence function of the entire system.

Referring to Figure 3, the circuit layout of the present utility model and its operation principle is as follows: the "television control card" and "DVB control card" are mutually exclusive. Only one of the cards can be inserted at one time. The card and main board are connected via the $I^2C$ bus. The "television control card slot" and "DVB control card slot" are electrically connected to the circuit board through control lines for television function control. To make the description easier, both cards are described together as one combined card.

The signal input (RF) port of the "television high frequency head" receives the high frequency carrier signal from the open television antenna or cable television line. It selects signal VHF1 or VHF2 to display the received channel of the frequency band of the ST9291 microcontroller on the "television control card" or the 8255A "DVB control card" I/O expansion port. Based on the modulated voltage input on the "modulation voltage" (VTURE) control input port, modulation of the television channel is performed. The modulation locked television radio signal is mixed and filter to generate the television IF signal (IF). The IF signal passes through a surface acoustic wave filter before being input into the IF integrated STV8223B. The IF integrated STV8223B automatic gain threshold control comes from the ST9291 microcontroller of the "television control card" or the automatic gain control (AGC) pin 8255A "DVB control card" I/O expansion port. The television's audio system mode is selected by the input from the "audio system mode control" (Audio std1 and Audio std2). The video frequency signal of the external AV input and the AV signal from the television-modulated high frequency carrier wave are switched at the IF integrated STV8223B. This switching is controlled by the "TV/AV" control pin. The demodulated video frequency signal from the IF integrated STV8223B or the video frequency signal from the AV input port are tied to pin **11** of the IF integrated STV8223B to the video frequency / hue integrated STV2118B to be decoded into the three primary color image signal for a television. The video frequency / hue integrated STV2118B contains two image input ports. The signal can be input on pin **20** as a Y/C signal, or as a full television DVBS signal form, or as the three primary color

RGB signal form on pins **12**, **13**, and **14**, depending on the register setting of the video frequency / hue integrated STV2118B. The register setting is set by the control data of the $I^2C$ bus port (SDA and SCL). The $I^2C$ bus control data is provided by the ST9291 microcontroller of the "television control card" or from the STi5500 microcontroller of the "DVB control card". Thus, the input/output of the video frequency / hue integrated STV2118B is directly controlled by the application software of the microcontroller. Pin **36** of the video frequency / hue integrated STV2118B outputs the oscillation signal to drive the output and generate a drive the high voltage required by the CRT filament, rail, collector, and /6 cathode, as well as the current for CRT coil deflection. Pin **35** of the video frequency / hue integrated STV2118B outputs the oscillation signal to the oscillate the oscillation output to generate the needed current for the CRT field deflection coil. The power for the video frequency / hue integrated STV2118B is provided from output pin 6 of the +15 V regulated power source integrated TDA8138A in the television set switched power supply; obtained from a three-port regulated power supply. Pin **6** of the regulated power source integrated TDA8138A outputting +12 V is determined by the POWER ON/OFF control pin of the ST9291 microcontroller in the "television control card" or the 8255A "DVB control card" I/O expansion port. As long as the ST9291 microcontroller in the "television control card" or the 8255A "DVB control card" I/O expansion port receives a power on command from the end-user, the POWER ON/OFF control pin is in an ON state and power is supplied to the video frequency / hue integrated STV2118A, providing the horizontal and field oscillation signals. Thus, the television is in an ON state. The onboard keys receive second-circuit key scan signals (KS4 and KS5) from the ST9291 microcontroller in the "television control card" or the 8255A "DVB control card" I/O expansion port and send key state information of the key scan output (KS1, KS2, and KS) to the ST9291 microcontroller in the "television control card" or the 8255A "DVB control card" I/O expansion port. The STi5500 microcontroller of the ST9291 microcontroller in the "television control card" or the 8255A "DVB control card" I/O expansion port receives the television circuit signal and, through determinate processing, generates a corresponding control signal that, after passing though electromagnetic inference isolation, controls the operation of the corresponding circuit. The control signal can be sent through the I/O port or the $I^2C$ bus (SDA and SCL). The remote control receiver receives control code from the infrared remote control. The interrupt port of the STi5500 microcontroller of the ST9291 microcontroller in the "television control card" or the 8255A "DVB control card" I/O expansion port enables the remote control procedure and receives the remote control commands from the /7 interrupt of the process. The DVB high frequency head receives high frequency carrier wave signals from an LNB on an antenna, received from a satellite. Through modulation and mixing and then quadrature phase shift keying (QPSK) demodulation, the image is restored according to the transmission stream (TS) as defined by the Moving Picture Experts Group (MPEG2). The control signals needed by the DVB high frequency processor are set on the $I^2C$ bus (SDA and SCL) by the STi5500 microcontroller of the "DVB control card". The +22 V power of the LNB is supplied by the television power switch. The KM416V1000C random storage device is a 1 M x 16 bit SDRAM, used by the STi5500 microcontroller of the "DVB control card" to decode MPEG2 images. The read-only DD28F032SA storage device is a 2 M x 16 bit FLASH ROM, used to store application software. The 24C256 storage device is a E$^2$PROM storage device, used to sure DVB and television channel information. The 24C256 storage device is controlled by the I$^2$C bus (SDA and SCL). The 8255A "DVB control card" I/O expansion port and the ST9291 microcontroller in the "television control card" have compatible pin-outs on the main board of which it is directly connected. The STi5500 microcontroller of the "DVB control card" controls the entire television circuit through the 8255A I/O expansion port. Thus, when a television set that supports receiving DVB functionality is manufactured, the ST9291 microcontroller for controlling the television and the 24C08 storage device are not needed.

The STi5500 microcontroller of the "DVB control card" is a large-scale integrated circuit. It includes a ST20, a 32 bit RISC high-speed processor used to control the operation of the entire system, including the 8255A I/O expansion port and a MPEG decoder to receive a processed TS stream from the DVB high frequency head, of which the decoded video image data is sent to an encoder to generate a three primary color image RGB signal, which is sent to the video frequency / hue integrated STV2118B. /8

The STi5500 microcontroller of the "DVB control card" uses a 40 MHz clock, which generates a great amount of electromagnetic interference for the analog part of a television signal. The control bus, data bus, and address bus connecting the DD28F032SA read-only storage device and

KM416V1000C random storage device outside the STi5500 microcontroller of the "DVB control card" also transfer data at very high speeds and are especially susceptible to electromagnetic interference from the television set. The CRT used in a television set in and of itself is also a source for a great amount of interference. Its power switch uses a switch pulse drive, as well as the output pole. The peak to peak voltage value generated by the pulse can reach 1000 V (14 kHz). This switch pulse signal is a very wide band in the frequency region. Such a high voltage broad band switch signal is extremely dangerous for the "DVB control card". The actual implementation of this preferred embodiment exhibited such behavior. If effective measures are not take, the data in the STi5500 microcontroller of the "DVB control card" and the DRAM and $E^2$PROM in the ST9291 microcontroller in the "television control card" will be corrupt and cause abnormal operation of the program which may damage the device. Additionally, a spark may occur on the cathode of the television set CRT. When a spark occurs, it can cause severe electromagnetic interference and, in the same manner, can affect the normal operation of the program. Isolation measures were taken to prevent the affects of these two issues. One was to add a LC isolation filter between the card and the main board to isolate the electrical interference. The other was to enclose the card in a metal case to shield it from electromagnetic field interference.

To reduce costs, the power for the "DVB control card" is provided by the switch power supply of the television set. A 7 V coil power supply is rectified and passes through an integrated PQ3RD3 regulated voltage to provide 3.3 V of regulated power for the STi5500 microprocessor in the "DVB control card". The LNB power is supplied by a single +22 V power supply. The power supply is connect to a port on the "D"B control card". A LC is used for isolation. /9

Referring to Figure 4, the I/O pore expansion circuit of the present utility model is implemented based on the following principles. The KM4161000C DRAM, DD28F032SA flash ROM, and 8225A I/O expansion use the data bus (data bus 0 - data bus 7), address bus (address A0 and A1), and some control lines. The KM4161000C DRAM port is determined by the horizontal port and vertical ports 0 and 1. The DD28F032SA flash ROM storage device port is determined by $\overline{CE3}$. The 8255A expansion port is determined by $\overline{CE1}$. Thus, depending the data for different addresses corresponds to a chip enable signal the provide the accurate search address for the aforementioned elements outside the STi5500. Because the STi5500 microprocessor in the "DVB control card" does not include the pins required for write operations of the I/O expansion 8255A , the $\overline{OE}$ pin of the STi5500 microprocessor in the "DVB control card" is used as a replacement. In this manner can the I/O port of the I/O expansion 8255A perform write operations. Referring to Figure 5, the EMC port is formed from a LC. The inductor provides isolation capabilities to high frequency signals to prevent high frequency interference and the capacitor offer a grounding path for high frequency signals to absorb interfering high frequency signals. This LC network is the EMC measure for this card.

Referring to Figure 6, when the "television control card" of the present utility model is used, when the "program source" button is pressed, the program will switch as shown between the television 20 and the external A/V port 21.

Referring to Figure 7, when the "DVB control card" of the present utility model is used, when the "program source" button is pressed, the program will switch as shown between the television 30 and the external A/V port 31, and the digital television broadcast 32. Thus, enabling the user to watch all programs with only one set of device wires and one remote control.

DESCRIPTION OF THE DIAGRAMS

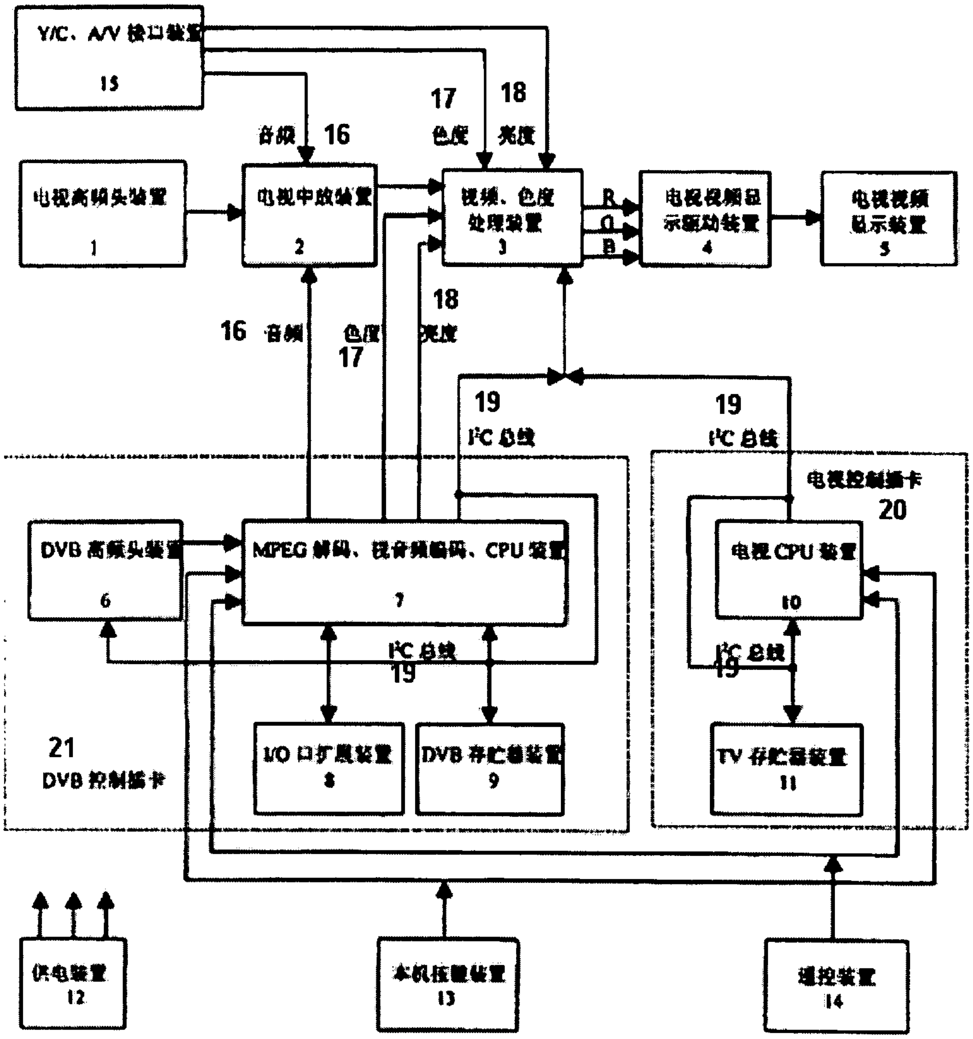

Figure 1

Figure 1 Key:
1. Television high frequency head device
2. Television IF device
3. Color and hue processing device
4. Television video frequency display driver device
5. Television video frequency display device
6. DVB high frequency head device
7. MPEG decoder, A/V encoder, and CPU device
8. I/O port expansion device
9. DVB storage device
10. Television CPU device
11. TV storage device

12. Power supply device
13. On-board key device
14. Remote control device
15. Y/C and A/V port device
16. Audio
17. Hue
18. Brightness
19. $I^2C$ bus
20. Television control card
21. DVB control card

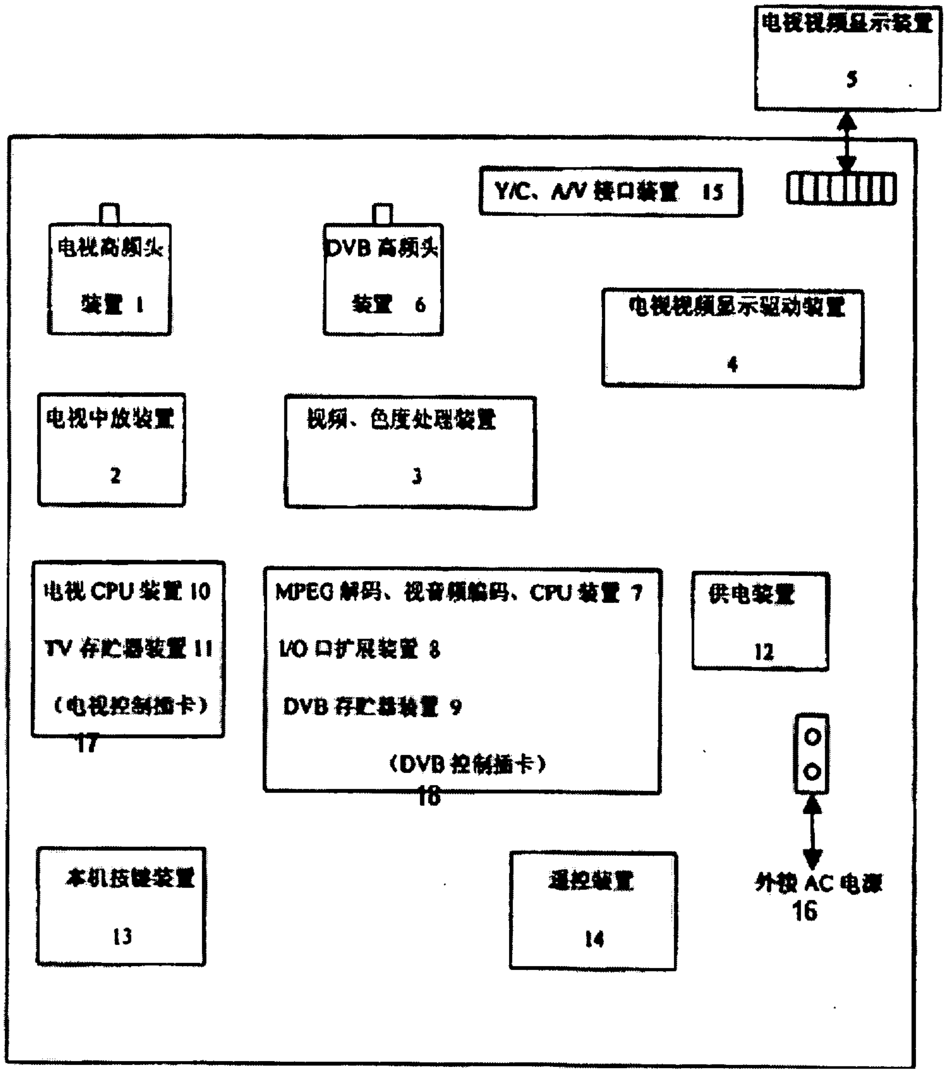

Figure 2

Figure 2 Key:

1. Television high frequency head device
2. Television IF device
3. Color and hue processing device
4. Television video frequency display driver device
5. Television video frequency display device
6. DVB high frequency head device
7. MPEG decoder, A/V encoder, and CPU device
8. I/O port expansion device
9. DVB storage device
10. Television CPU device
11. TV storage device
12. Power supply device
13. On-board key device

14. Remote control device
15. Y/C and A/V port device
16. External power supply
17. Television control card
18. DVB control card

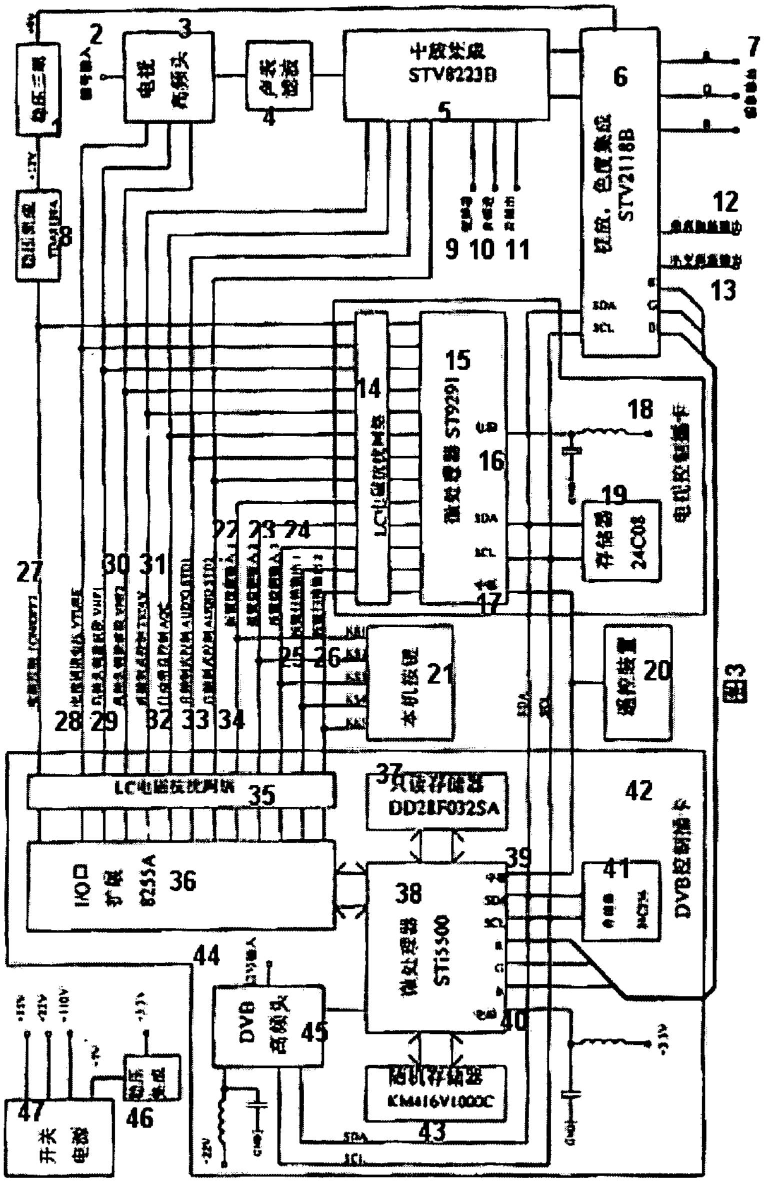

Figure 3

Figure 3 Key:
1. Three port regulated power
2. Signal input
3. Television high frequency head
4. Surface acoustic wave filter
5. IF integrated STV8223B
6. Video frequency, hue integrated STV2118B
7. Image output
8. Regulated power integrated TDA8138A
9. Video frequency input

10. Audio frequency input
11. Audio frequency output
12. Vertical oscillation output
13. Horizontal oscillation output
14. LC television interference prevention network
15. ST9291 microcontroller
16. Vcc
17. Int
18. Television control card
19. 24C08 storage device
20. Remote control device
21. Onboard keys
22. Key check input 1
23. Key check input 2
24. Key check input 3
25. Key scan output 1
26. Key scan output 2
27. Power supply control (ON/OFF)
28. Television power modulation voltage (VTURE)
29. High frequency head modulation band (VHF1)
30. High frequency head modulation band (VHF2)
31. A/V mode control (TV/AV)
32. Automatic gain control (AGC)
33. Audio frequency mode control (AUDIO STD1)
34. Audio frequency mode control (AUDIO STD2)
35. LC electromagnetic interference prevention network
36. I/O port expansion 8255A
37. DD28F032SA read-only storage device
38. STi550 microcontroller
39. Int
40. Vcc
41. 24C256 storage device
42. DVB control card
43. KM416V1000C random storage device
44. Signal input
45. DVB high frequency head
46. Integrated regulated voltage
47. Power switch

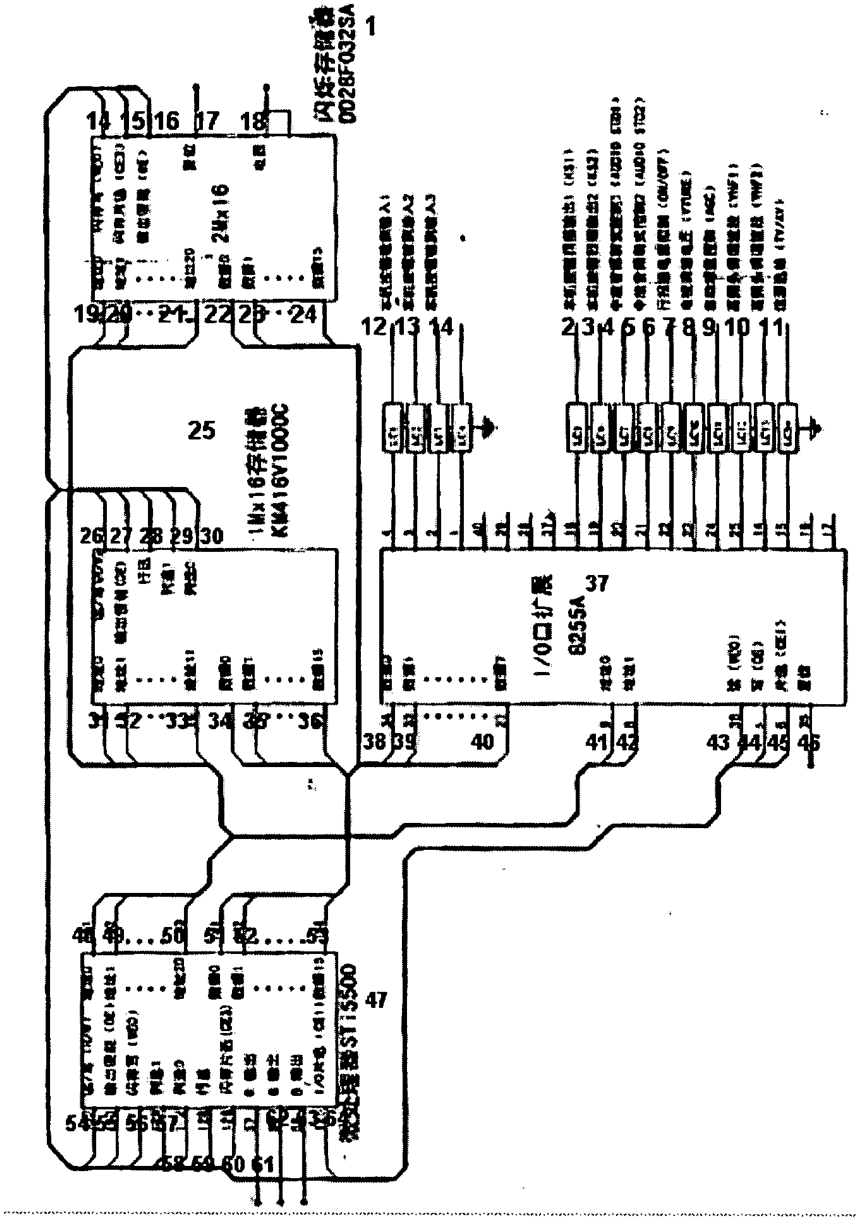

Figure 4

Figure 4 Key:

1. DD28F032SA flash storage device
2. On-board key scan output 1 (KS1)
3. On-board key scan output 2 (KS2)
4. IF audio frequency mode control 1 (AUDIO STD1)
5. IF audio frequency mode control 2 (AUDIO STD2)
6. On/off power control (ON/OFF)
7. Television modulated voltage (VTURE)
8. Automatic gain control (AGC)
9. High frequency head modulation band (VHF1)
10. High frequency head modulation band (VHF2)

11. Signal source select (TV/AV)
12. On-board key check input 1
13. On-board key check input 2
14. On-board key check input 3
14. Flash write (WEO)
15. Flash chip select (CE3)
16. Output enable (OE)
17. Reset
18. Vcc
19. Address 0
20. Address 1
21. Address 20
22. Data 0
23. Data 1
24. Data 15
25. KV416V1000C 1 M x 16 bit storage device
26. Read/write (R/W)
27. Output enable (OE)
28. Column select
29. Row select 1
30. Row select 0
31. Address 0
32. Address 1
33. Address 11
34. Data 0
35. Data 1
36. Data 15
37. I/O port expansion 8255A
38. Data 0
39. Data 1
40. Data 7
41. Address 0
42. Address 1
43. Read (WEO)
44. Write (OE)
45. Chip select (CE1)
46. Reset
47. STi550 microcontroller
48. Address 0
49. Address 1
50. Address 20
51. Data 0
52. Data 1
53. Data 15
54. Read/write (R/W)
55. Output enable (OE)
56. Flash write (WEO)
57. Row select 1
58. Row select 0
59. Column select

60. Flash chip select (CE3)
61. R output
62. G output
63. B output
64. I/O chip select (CE1)

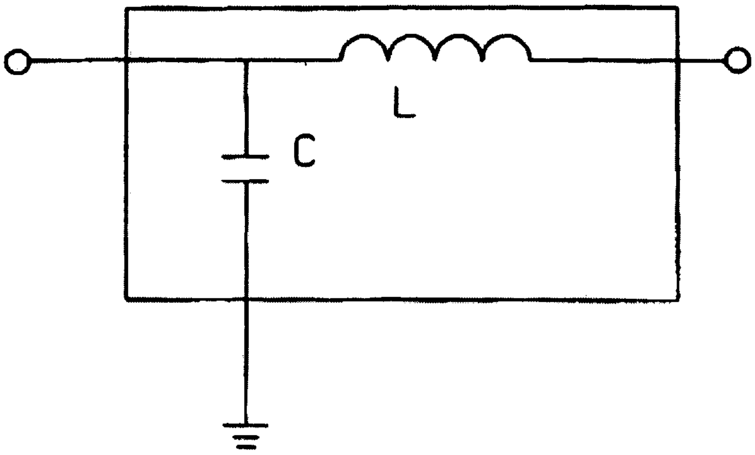

Figure 5

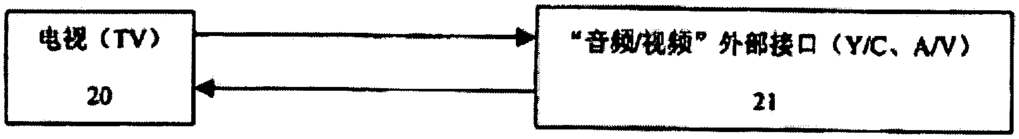

Figure 6

Figure 6 Key:
20. Television (TV)
21. A/V external port (Y/C, A/V)

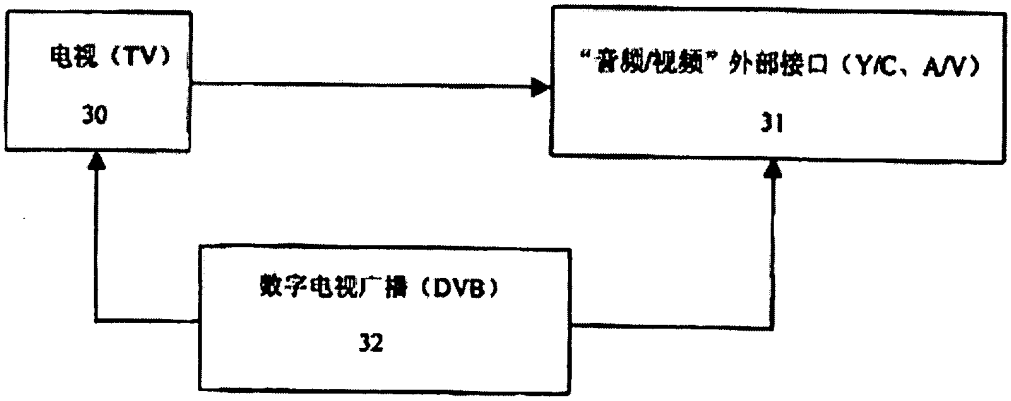

Figure 7

Figure 6 Key:
30. Television (TV)

31. A/V external port (Y/C, A/V)
32. Digital television broadcast (DVB)